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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
NATNAEL, PAULOS M

ART UNIT	PAPER NUMBER
2614	

DATE MAILED: 11/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/191,629	TRAN ET AL.	
	Examiner	Art Unit	
	Paulos M. Natnael	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-33 and 48-52* is/are allowed.

6)☒ Claim(s) *1,3-6,34-38 and 40-46, 53-61* is/are rejected.

7)☒ Claim(s) *2,7,39 and 47* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. Applicant is required to correct the requested amendment to specification. At page 5, line 4, there is no "87" to be replaced by "81".

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims **1, 3-5, 34-37** are rejected under 35 U.S.C. 102(e) as being anticipated by Swan, U.S. Pat. No. 6,304,297.

4.

Considering claim **1**, Swan discloses all claimed subject matter, note;

a) the claimed method of storing incoming digital television data in the first frame buffer is met by the back section 30 of frame buffer 14, Fig.1; (col. 3, lines 1-4 and col. 4, lines 32-35)

b) the claimed method of reading outgoing digital television data from the second frame buffer is met by the front section 32 of frame buffer 14, Fig.1; (col. 3, lines 1-4 and col. 4, lines 32-35)

c) the claimed method of monitoring refresh of a display device coupled to the system is met by the disclosure that "...the display driver 16 is reading the data from the frame buffer 14 at the refresh rate and the video processor 12 is writing the data at the display update rate, where the display update rate and the refresh rate match." (Col. 3, lines 19-23);

d) the claimed method of transmitting the outgoing digital television data in the second frame buffer to the display device when a programmed position of the display device is refreshed is met by the "display driver 16, which provides the display data 34 to a computer monitor or similar device" (col. 3, lines 15-16) and the disclosure that "...the display driver 16 is reading the data from the frame buffer 14 at the refresh rate and the video processor 12 is writing the data at the display update rate, where the display update rate and the refresh rate match." (Col. 3, lines 19-23)

Considering claim **3**, the claimed method of detecting whether the outgoing digital television data is stored in the first frame buffer or the second frame buffer is met by the disclosure that "the video processor 12 causes a frame, or field, of video data 28 to be stored in the back section 30 of frame buffer 14." (Col. 2, lines 66 to Col. 3, line 1)

Considering claim **4**, the claimed method of monitoring step comprising the step of monitoring a horizontal sync and a vertical sync of the display device, is inherent because, as Swan discloses, "....techniques have been developed to increase the synchronization between the display update rate of video images and the refresh rate of computer monitors." (Col. 1, lines 60-62)

Considering claim **5**, the claimed wherein the outgoing digital television data transmitted to the display device comprises a frame is inherent, because the data is written and read in frames by the frame buffers.

Considering claim **34**, Swan discloses all claimed subject matter, note;

a) the claimed first storing means for storing the incoming digital television data and the outgoing digital television data in an alternating manner is met by frame buffer 14, Fig.1;

b) a second storing means for storing the outgoing digital television data and the incoming digital television data in an alternating manner is met by the frame buffer 14, Fig.1;

c) the claimed a monitoring means for monitoring refresh of a display device is met by video processor 12, Fig.1;

d) the claimed a transmitting means for transmitting the outgoing digital television data in a storing means to the display device when a programmed position of the display device is refreshed, is met by the "display driver 16, which provides the display data 34 to a computer monitor or similar device" (col. 3, lines 15-16) and the disclosure that "...the display driver 16 is reading the data from the frame buffer 14 at the refresh rate and the video processor 12 is writing the data at the display update rate, where the display update rate and the refresh rate match." (Col. 3, lines 19-23

Considering claim **35**, a means for reading the outgoing digital television data from a storing means is met by display driver 16, which "is reading the data from the frame buffer 14..." (Col. 3, lines 16-17)

Considering claim 36, the claimed means for monitoring a horizontal sync and a vertical sync of the display device is inherent because, as Swan discloses, "....techniques have been developed to increase the synchronization between the display update rate of video images and the refresh rate of computer monitors." (Col. 1, lines 60-62)

Considering claim **37**, the claimed detecting means for detecting whether the outgoing digital television data is stored in the first storing means or the second storing means is met by video processor 12, FIG.1;

5. Claims **57-61** are rejected under 35 U.S.C. 102(e) as being anticipated by **Johnson**, U.S. Pat. No. 6, 330,038.

Considering claim **57**, Johnson discloses all claimed subject matter, note;

a) the claimed digital television/local bus interface logic for passing decoded digital television data is met video port 150, FIG.4;

b) the claimed a graphics controller for receiving the decoded digital television data over a local bus from the digital television/local bus interface logic is met graphics controller 154, FIG.4;

c) the claimed a display device for receiving the decoded digital television data from the graphics controller is met by Monitor 32 via VGA to Monitor interface 158.

Considering claim **58**, the claimed wherein the local bus comprises a peripheral component interconnect (PCI) bus is met by bus 108, Fig.3;

Considering claim **59**, the claimed a core logic for receiving the decoded digital television data from the digital television/local bus interface logic and passing the decoded digital television data to the graphics controller is met by video port 150, Fig.4;

Considering claim **60**, the claimed digital television decoder for providing decoded digital television data to the digital television/local bus interface logic is met by video decoder 146, FIG.4;

Considering claim **61**, the claimed digital television tuner for providing encoded digital television data to the digital television decoder is met by the disclosure that the A/V sub system 52 comprises two TV tuners, FIG.2;

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims **6 and 38** are rejected under 35 U.S.C. 103(a) as being unpatentable over Swan, U.S. Pat. No. 6,304,297 in view of the Admitted Prior Art (APA).

Considering claim **6**, Swan discloses all claimed subject matter, except for;

The claimed method of transmitting the outgoing digital television data over a peripheral component interconnect (PCI) bus;

Regarding claim 6, Swan does not specifically disclose the PCI bus, however, Examiner takes Official Notice here in that the PCI bus connecting peripheral components or devices is well known in the art as the APA shows in FIG. 1 and therefore, would have been obvious to the skilled in the art.

Considering claim **38**, see rejection of claim 6;

8. Claims **40, 42-46** are rejected under 35 U.S.C. 103(a) as being unpatentable over Bril et al., U.S. Pat. No. 6,118,413.

Considering claim **40**, Bril discloses the following claimed subject matter, note;

a) the claimed local bus is met by system bus 230, Fig. 2;

b) the claimed graphics controller coupled to the local bus is met graphics controller 210, Fig. 2;

c) the claimed display device for receiving outgoing digital television data from the graphics controller is met by TV 292 (or DSTN 270), Fig. 2;

Except for;

d) the claimed digital television/local bus interface logic coupled to the local bus for storing incoming digital television data and the outgoing digital television data and selectively providing the outgoing digital television data over the local bus to the graphics controller when a programmed position of the display device is refreshed.

Regarding d), Bril does not specifically disclose a separate I/f logic. However, Bril discloses a display memory 220 and ½ frame buffer 240 storing data and selectively sending video data to the graphics controller 210. Therefore, it would have been obvious to the skilled in the art at the time the invention was made that would be implemented by the display memory 220 and ½ frame buffer 240 performing the functionality of the claimed I/F logic, and the display device with its independent refresh rate.

Considering claim **42**, the claimed digital television decoder for providing incoming television data to the digital television/local bus interface logic;

Regarding claim 42, Bril doesn't disclose a decoder. However, Examiner takes Official Notice that the television decoder is well known in the art, and thus would have been obvious to the skilled in the art at the time the invention was made to provide the decoder and modify the system of Bril et al.

Considering claim **43**, the claimed digital television tuner for providing incoming digital television data to the digital television decoder.

Regarding claim 43, see rejection of claim 42.

Considering claim **44**, wherein the graphics controller provides a feedback signal to the digital television/local bus interface logic to indicate whether the programmed position of the display device is refreshed.

Regarding claim 44, see rejection of claim 40 (d).

Considering claim **45**, the claimed wherein the feedback signal comprises a horizontal sync and a vertical sync of the display device is inherent, because any video processing system would have horizontal sync and vertical sync signal in order to properly function or operate.

Considering claim **46**, the claimed wherein the local bus comprises a peripheral component interconnect (PCI) bus.

Regarding claim 46, Swan does not specifically disclose the PCI bus, however, Examiner takes Official Notice here in that the PCI bus connecting peripheral components or devices is well known in the art as the APA shows in FIG. 1 and therefore, would have been obvious to the skilled in the art.

9. Claim **41 is** rejected under 35 U.S.C. 103(a) as being unpatentable over Bril et al., U.S. Pat. No. 6,118,413 in view of the Admitted prior art (APA).

Considering claim **41**, the claimed a core logic coupled between the local bus and the graphics controller.

Bril doesn't specifically disclose a core logic. However, the core logic utilized in display devices is well known in the art. The APA discloses a core logic 10. Therefore, it would have been obvious to the skilled in the art to provide a core logic 10 and modify the reference of Bril in order to control the flow of data between the local bus and the graphics controller.

10. Claims **53-56** are rejected under 35 U.S.C. 103(a) as being unpatentable over Emelko, U.S. Pat. No. 6,122,010 in view of Wilson et al., U.S. Pat. No. 6,037,981.

Considering claim **53**, Emelko discloses the following claimed subject matter, note;

a) receiving encoded digital television data is met by the input from A/D 306 to Control Unit 320, Fig.12;

b) the claimed method of decoding the encoded digital television data to generate decoded digital television data is met by Control Unit 320, Fig.12;

Except for;

c) the claimed method of sending the decoded digital television data over a local bus of the computer system to a graphics controller;

Regarding c), Emelko doesn't disclose a graphics controller. Emelko however discloses that the control unit 320 communicates with FIFO 308 and with computer system 310 (via PC

bus 312)." (Col. 10, lines 23-25) Emelko further discloses that "the decoded data may be displayed by computer system 310 on a monitor, in a case where the decoded data represents visual data." (Col. 11, lines 4-7)

Wilson et al. disclose a method and apparatus for using digital television as remote personal computer display. Wilson discloses the personal computer system 100 including a graphics controller 113.

Accordingly, therefore, it would have been obvious to one of ordinary skill in the art to modify the system of Emelko by providing the graphics controller of Wilson in view of their closely related performance and the resulting expectation of similar output values of displaying graphics on monitor or screen.

Considering claim **54**, the claimed wherein the local bus comprises a peripheral component interconnect (PCI) bus;

Regarding claim 6, Swan does not specifically disclose the PCI bus, however, Examiner takes Official Notice here in that the PCI bus connecting peripheral components or devices is well known in the art as the APA shows in FIG. 1 and therefore, would have been obvious to the skilled in the art.

Considering claim 55, sending the decoded digital television data from the graphics controller to a display device.

Regarding claim 55, see rejection of claim 53 (c).

Considering claim 56, the claimed method of sending decoded digital television data over the local bus to core logic and from the core logic to the graphics controller.

Regarding claim 56, see rejection of claim 53 (c).

Response to Arguments

11. Applicant's arguments filed August 9, 2002 concering claim 1-6 and 34-37 have been fully considered but they are not persuasive.

Applicant's Arguments

a) Transmitting the video data out of the front section 32 of frame buffer 14 is not based on when a programmed position of a display device is refreshed.

Examiner's Response

a) Swan teaches that "As is known, the video graphics circuitry prepares frames of video images for display on the computer monitor. In general, the video graphics circuitry produces a frame's worth of video data at a rate that is dependent upon the refresh rate of the computer monitor. [emphasis added] For example, if the refresh rate is 60 hertz, the video graphics circuitry must

produce and store a frame of video data in a frame buffer once every 1/60th of a second. If the refresh rate of the computer monitor is 75 Hz, 90 Hz, or greater, the video graphics circuit must produce the frame of video data in even less time." (Col. 1, lines 20-30)

Swan discloses that the display driver 16, "provides the display data 34 to a computer monitor or similar device" (col. 3, lines 15-16) and that "...the display driver 16 is reading the data from the frame buffer 14 at the refresh rate and the video processor 12 is writing the data at the display update rate, where the display update rate and the refresh rate match." (Col. 3, lines 19-23)

Swan further teaches a video rate adjusting module 16 that calculates the adjustment value so that the video processor would be able to manipulate display update rate. Thus, argument is not persuasive.

Allowable Subject Matter

12. Claims **8-33, 48-52** are allowed.

13. Claims **2,7, 39, 47** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose digital television/local bus interface logic comprising,

storing the incoming digital television data in the second frame buffer, and reading the outgoing digital television data from the first frame buffer, as in claim 2;

Digital television/local bus interface logic coupled to the local bus; a first frame buffer for storing the incoming digital television data and the outgoing digital television data in an alternating manner; second frame buffer for storing the outgoing digital television data and the incoming digital television data in an alternating manner; memory controller for storing the incoming digital television data to one frame buffer and reading the outgoing digital television data from another frame buffer; digital television interface for receiving incoming digital television data, as in claim **8**;

A digital television interface for receiving incoming digital television data; a first frame buffer for storing the incoming digital television data and the outgoing digital television data in an alternating manner; a second frame buffer for storing the outgoing digital television data and the incoming digital television data in an alternating manner; a memory controller for storing the incoming digital television data to one frame buffer and reading the outgoing digital television data from another frame buffer on a first portion of a refresh of a display device and transmitting the outgoing digital television data in the one frame buffer to the display device on a second portion of the refresh of the display device, as in claim 17;

A first interface means for receiving incoming digital television data; a second interface means for transmitting outgoing digital television data; first buffer means for storing the incoming digital television data and the outgoing digital television data in an alternating manner; a second

buffer means for storing the outgoing digital television data and the incoming digital television data in an alternating manner; controller means for storing the incoming digital television data to one buffer means and reading the outgoing digital television data from another buffer means, as in claim **25.**

Wherein a refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data, as in claims **39 and 47**;

A memory controller for storing the first incoming digital television data stream to the first frame buffer or the second frame buffer and reading the first outgoing digital television data stream from the second frame buffer or the first frame buffer on a first portion of a refresh of a display device, storing the second incoming digital television data stream to the third frame buffer or the fourth frame buffer and reading the second outgoing digital television data stream from the fourth frame buffer or the third frame buffer on the first portion of the refresh of the display device, transmitting the first outgoing digital television data stream to the display device on a second portion of the refresh of the display device, and transmitting the second outgoing digital television data stream to the display device on the second portion of the refresh of the display device, as in claim **48.**

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Paulos Natnael** whose telephone number is **(703) 305-0019.** The examiner can normally be reached on **Monday through Friday** from **6:30 a.m.** to **3:00 p.m.**

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **John Miller,** can be reached on **(703)305-4795.**

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is **(703)305-3900.**

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314, (for formal communications intended for entry)

or:

(703)872-9314 (for informal or draft communications, please label "PROPOSED" OR "DRAFT").

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, V.A. Sixth Floor (Receptionist).

Paulos M. Natnael

November 1, 2002

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